REMARKS/ARGUMENTS

Claims 1-30 are pending in this application. In response to the prior art rejections, claims 1, 11, and 21 have been amended. Claim 13 has been amended to correct a typographical error. Claims 23-30 were previously added. It is respectfully submitted that no new matter has been added.

Applicant respectfully requests that the above-identified application be reconsidered in view of the following remarks.

Claim Rejections under 35 U.S.C. §102(b)

Claims 1-30 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,210,829 to Haim Bitner ("Bitner"). Bitner discloses a tape drive with an electronic buffer that temporarily stores data transferred between the host computer and the tape driver's magnetic tape. During a write transaction, in which the host computer sends data to the tape for storage, the buffer receives that data sent over the system bus by the host computer, and it temporarily stores the data until the tape mechanism has ramped up to its write velocity. The buffer has an adjustable threshold, otherwise known as a "watermark," which determines the level of data that must be present in the buffer before the mechanical assembly of the tape drive will begin to ramp the tape up to its write velocity. When the write velocity is achieved, the data in the buffer is transferred onto the tape, and the buffer is emptied so that it may receive additional data. (*See* Abstract).

These rejections are traversed, in part, because the cited reference fails to teach or suggest features of the presently claimed invention for loading a memory buffer as recited in the claims. For example, the cited reference fails to teach or suggest a memory buffer coupled to a memory controller, wherein said memory controller can receive an advance indication of a memory service interruption. Moreover, the cited reference fails to teach or

suggest that based.at least in part on the received advance indication of the memory service interruption, the watermark can be modified.

According to an embodiment of the present invention, a memory controller receives a memory service interruption advance signal that can provide advance warning that a memory service interruption will occur. In response to this advance warning, the watermark value is modified. The Bitner system differs. In Bitner, the watermark is modified after such an interruption occurs. (*See* Bitner, col. 4 lines 1-7). In other words, a major difference from Bitner is that in the presently claimed invention, the watermark value is pre-emptively modified prior to a memory service interruption. Accordingly, claims 1, 11, and 21 have been rewritten to further bring out this feature of the present invention.

In rejecting independent claim 15 and claims 16-18, which ultimately depend from independent claim 15, the Office Action states that Bitner teaches an apparatus to control the loading of a memory buffer, comprising: a memory buffer (Examiner cites to fig. 1 element 34); and a memory controller, coupled to said memory buffer (Examiner cites to fig.1 element 32 and col. 6 lines 59-68 and col. 7 lines 1-2, stating "wherein the controller 32 contains the buffer 34"), including a watermark register (Examiner cites to fig. 4 write cycle #8-12 and col. 14 lines 29-61 and col. 15 lines 1-14, stating "wherein the watermark is adjustable to maximize the availability of the buffer to receive data from the host computer 20 therefore it is obviously the controller having a watermark register"); a first register, coupled to said watermark register, to store a first watermark value (Examiner cites to fig. 4 write cycle #9 and col. 14 lines 29-61 and col. 15 lines 1-14, stating "wherein assumed that the memory buffer 34 has a first watermark value at the write cycle #9; therefore, it is obviously the controller has a first register); and a second register, coupled to said watermark register, to store a second watermark value (Examiner cites to fig. 4 write cycle #11 and col. 14 lines 29-61 and col. 15 lines 1-14, stating "wherein the watermark is advanced to a second

watermark value 430 Kb; therefore, it is obviously the controller has a second register"). Applicant respectfully disagrees. Bitner does not teach an apparatus comprised of a memory controller coupled to a memory buffer, but instead concerns a "tape controller" which contains within it a buffer. (*See* Bitner, col. 6 lines 59-61 and Fig. 1). Furthermore, the memory controller of the presently claimed invention and Bitner's tape controller may perform different functions. In the presently claimed invention, the memory controller controls the pre-loading of the memory buffer, whereas in Bitner, the tape controller initiates the tape drive's read/write operations, leaving the buffer to operate independently. (*See* Bitner, col. 6 lines 62-63 and col. 27 lines 11-14).

In rejecting independent claim 19 and claim 20, which ultimately depends from independent claim 19, the Office Action states that claim 19 is of similar scope as claim 15 and is therefore rejected under the same rational. The Office Action further states that Bitner also teaches a system to process video signals, the system comprising: a processor (Examiner cites to fig. 1); and memory, coupled to said processor (Examiner cites to fig. 1). Applicant respectfully disagrees by similar reasoning as claim 15 and claims 16-18.

In rejecting independent claim 23 and claims 24-27, which ultimately depend from independent claim 23, the Office Action states that claims 23 is of similar scope as claim 15 and is therefore rejected under the same rational. Applicant respectfully disagrees by similar reasoning as claim 15 and claims 16-18.

In rejecting independent claim 28 and claims 29-30, which ultimately depend from independent claim 28, the Office Action states that Bitner teaches an apparatus comprising: a video stream buffer (Examiner cites to fig. 1 elements 34, 26 and col. 25 lines 14-19, stating "wherein the buffer 34 can be a video stream buffer because the tape drive 26 also be implemented in other electromechanical devices") a memory controller to occasionally perform an operation causing a memory services interruption (Examiner cites to fig. 1 and

fig. 4 write cycle #9-10 and col. 14 lines 29-61, stating "wherein at the write cycle #9 the video stream buffer 34 receives a memory service interruption from the memory controller indicating no host stall occurred therefore the video stream buffer is advanced to higher level of buffer); and control logic coupled to said video stream buffer to maintain a first level of buffering in a first mode and to maintain a higher level of buffering prior to said memory controller performing said operation causing said memory service interruption (Examiner cites to fig. 4 write cycle #9-10 and col. 14 lines 29-61, stating "wherein the video stream buffer is advanced to a higher level of buffering prior to the memory performing the operation causing the memory device interruption). Applicant respectfully disagrees by similar reasoning as claims 15-20 and claims 23-27.

In view of the amendments and remarks above, reconsideration and withdrawal of the rejection of claims 1-30 under 35 U.S.C. § 102(b) is respectfully requested.

CONCLUSION

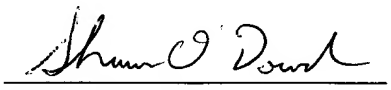
The Office Action rejected the remaining claims on analogous grounds. Because all remaining claims ultimately depend upon the independent claims, Applicant respectfully requests that the rejection of these claims be reconsidered. Accordingly, reconsideration and withdrawal of the rejection of claims 2-10, 12-14, 16-18, 20, 22, 24-27, 29, and 30 which ultimately depend from claims 1, 11, 15, 19, 21, 23, and 28, respectively under 35 U.S. C. §102(b) is respectfully requested.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

Dated: June 9, 2002

By: 

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